REMARKS

The following remarks are made in response to the Final Office Action mailed November 7, 2007. Claims 17-19, 22-25, and 29-31 were rejected. With this Response, claim 24 has been amended and new claim 40 has been added. Claims 17-19, 22-25, 29-31, and 40 remain pending in the application and are presented for reconsideration and allowance.

Claim Rejections under 35 U.S.C. § 102

The Examiner rejected claims 17-19, 22-25, and 29-31 under 35 U.S.C. § 102(b) as being anticipated by the Duff et al. GB Patent No. 2 002 157.

Independent claim 17 includes wherein the control device is configured to drive the oscillator such that the at least two generated output frequencies are alternated at an average frequency that is less than the at least two possible output frequencies. Independent claim 29 includes alternating the at least two generated output frequencies at an average frequency that is less than the at least two different output frequencies.

The Duff GB Patent does not teach or suggest the above limitations of independent claim 17 and independent claim 29. The Examiner specifically cites the Duff GB Patent at Page 2, lines 104-110 which states:

> By selectively opening and closing first switching means 3 and second switching means 6 for desired periods of time, a higher or lower average frequency (relative to that frequency normally supplied by divider 4 at output terminal 40) will appear at terminal 8.

This passage of the Duff GB Patent, however, does not disclose any statement regarding the frequency at which at least two output frequencies are alternated (i.e., the speed of switching between the output frequencies), such as defined in amended independent claims 17 and 29. Instead, the desired periods of time referred to in the above passage of the Duff GB Patent specifically refers to the desired periods of time that selected conditions are maintained based on selectively opening and closing first switching means 3 and second switching means 6.

The Duff GB Patent specifically refers to three conditions to produce either higher or lower average output frequencies. In the normal condition, if no change to the frequency is

desired from that which is normally supplied by divider 4, first switching means 3 will be closed and second switching means 6 will be open to allow the signal supplied to terminal 7 to pass through divider 4 and appear at terminal 8. See the Duff GB Patent at page 2, lines 110-119. The second condition is referred to as the "add pulse" condition and is produced by opening first switching means 3 and closing switching means 6 to thereby have the signals appearing at terminal 7 bypass divider 4 and appear directly at terminal 8. See the Duff GB Patent at page 2, lines 120-125. The GB Patent at page 2, lines 125-128 specifically states that "this add pulse condition may be maintained for any desired period of time, thereby adjusting the average frequency appearing at terminal 8 upward." The third condition is referred to as the "subtract pulse" condition and is achieved by opening both first switching means 3 and the second switching means 6 for a selected time, such that no pulses will be transmitted from terminal 7 to terminal 8 during this selected time. See GB Patent at page 3, lines 28-46. The subtract pulse condition can be used to cause the average frequency appearing at terminal 8 to be less than that normally supplied. In view of the above, it is clear that the desired periods of time and the selected times referred to in these passages refers to the period of time the normal condition, the add pulse condition, and/or the subtract pulse condition are maintained based on selectively opening and closing switching means 3 and second switching means 6.

The Duff GB Patent does specifically refer to percentages at which the circuit shown in Figure 1 is operated in one of the normal condition, add pulse condition, or subtract pulse condition to obtain a either higher or lower time-averaged frequency appearing at terminal 8.

As to the speed of switching between the normal condition and the add pulse condition or between the normal condition and the subtract pulse condition, the Duff GB Patent at page 3, lines 22-27 states:

> By more rapidly switching the circuit shown in Figure 1 between the normal condition and the add pulse condition, the instantaneous frequency appearing at terminal 8 will more closely approach the desired average frequency over progressively shorter time periods.

This passage of the Duff GB Patent explicitly recommends employing a high switching frequency in switching between the normal condition and the add pulse condition and therefore teaches away from the control device being configured to drive the oscillator such that the at least two generated output frequencies are alternated at an average frequency that is less than the at least two possible output frequencies, such as recited in independent claim 17 and from alternating the at least two generated output frequencies at an average frequency that is less than the at least two different output frequencies as recited in independent claim 29.

Thus, the desired periods of time referred to by the Examiner do not refer to switching frequency and switching between the normal condition and either the add pulse condition or the subtract pulse condition, but rather to the amount of time the switches are in the normal condition compared to the amount of time the switches are in the add pulse condition or the subtract pulse condition to obtain either a higher or lower average output frequency. Applicant respectfully notes that this percentage of time in the normal condition as to compared to the percentage of time in either the add pulse condition or the subtract pulse condition may be obtained with a higher switching speed or a lower switching speed, and the Duff Patent at page 3, lines 22-27 specifically recommends employing a higher switching speed in switching between the normal condition and the add pulse condition.

In view of the above, independent claims 17 and 29 are not taught or suggested by the Duff Patent alone or in combination with the other cited references.

Furthermore, dependent claims 18-19 and 22-25 and new claim 40 further define patentability distinct amended independent claim 17 and dependent claims 30-31 further define patentability distinct amended independent claim 29. Therefore these dependent claims are also believed to be allowable.

In addition, Applicant points to the Examiners rejection of dependent claim 24. Independent claim 17 includes the limitations of the control device being configured to drive the oscillator such that an average value of the generated output frequencies over a certain time period is substantially the desired frequency and such that the at least two generated output frequencies are alternated at an average frequency that is less than the at least two possible output frequencies. Amended dependent claim 24 now further limits independent claim 17 to

include a frequency divider connected to the output of the oscillator and configured to cause the certain time period to be extended. Similarly, independent claim 29 includes driving the oscillator such that the average value of the at least two generated output frequencies over a certain time period corresponds to the desired frequency and alternating the at least two generated output frequencies and an average frequency that is less than the at least two different output frequencies. New dependent claim 40 further limits independent claim 29 to include dividing the frequency of the output signal generated by the oscillator to cause the certain time period to be extended. The limitations of amended dependent claim 24 and new dependent claim 40 are not taught or suggested by the Duff GB Patent. These limitations of the frequency divider or dividing the frequency to cause the averaging certain time period to be extended enables a smaller (i.e., slower) switching frequency of switching between the at least two output frequencies while still yielding a good approximation of the desired output frequency.

One example embodiment having the combination of limitations of independent claim 17 and amended dependent claim 24 and the combination of limitations of independent claim 29 and new dependent claim 40 is described at page 8 of the clean version of the substitute specification, which states that the frequency dividers cause the averaging period to be extended as illustrated in Figures 8A, 8B, and 8C of the present Specification. Figure 8A illustrates the time characteristic of the voltage of the control signal and the time characteristic of the frequency of the voltage of the signal f_{OUT} generated by the digitally controlled oscillator, and Figures 8B and 8C respectfully illustrate the time characteristic of the frequency and the voltage of the signal after the first and second frequency divider respectively to illustrate that the frequency dividers cause the averaging period to be extended. The example embodiment described at page 8 of the present Specification, specifically states that the relative frequency error at the output of the digitally controlled oscillator is 3.7% in the illustrated example and at the output of the second frequency divider, the relative frequency error is only 0.22%. In addition, the limitations of amended dependent claim 24 and new dependent claim 40 permit even slower switching frequencies, and slower switching frequencies are desirable as slower frequencies generally are easier to handle and control.

As stated in the above Examiner Interview Summary, Examiner Gannon agreed that dependent claim 18 is not taught by the Duff GB Patent for the reasons provided in the response to the non-final office action which are as follows. The Examiner, in the non-final office action, cited the Duff Patent and stated the Duff GB Patent teaches the control device being configured to drive the oscillator with the bit stream generator according to a delta-sigma principal, because the Examiner stated the controlled device of Duff operates in an analog to digital conversion principal, which is one form of delta-sigma conversion. Applicant, in response to the non-final office action, respectfully submitted, that this statement by the Examiner is not correct in that delta-sigma conversion is a special form of analog to digital conversion. Therefore, the Duff GB Patent does not teach or suggest the limitation of dependent claim 18 as agreed by the Examiner in the above summarized Examiner Interview.

Therefore, Applicant respectfully requests reconsideration and withdrawal of the 35 U.S.C. § 102(b) rejections to claims 17-19, 22-25, and 29-31, and request allowance of claims 17-19, 22-25, and 29-31 and new claim 40.

CONCLUSION

In view of the above, Applicant respectfully submits that pending claims 17-19, 22-25, 29-31, and 40 are in form for allowance and are not taught or suggested by the cited references. Therefore, reconsideration and withdrawal of the rejections and allowance of claims 17-19, 22-25, 29-31, and 40 are respectfully requested.

No fees are required under 37 C.F.R. 1.16(h)(i). However, if such fees are required, the Patent Office is hereby authorized to charge Deposit Account No. 50-0471.

The Examiner is invited to contact the Applicant's representative at the below-listed telephone numbers to facilitate prosecution of this application.

Any inquiry regarding this Amendment and Response should be directed to Patrick Billig at Telephone No. (612) 573-2003, Facsimile No. (612) 573-2005. In addition, all correspondence should continue to be directed to the following address:

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